

***Amendments to the Specification***

Kindly amend paragraph 1 as follows:

This application is a continuation of U.S. ~~Application~~ Patent No. ~~10/083,463~~ 6,639,430, filed February 27, 2002, which claims the benefit of U.S. Provisional Application No. 60/271,425, filed February 27, 2001, both of which are incorporated herein in their entirety by reference.

Kindly amend paragraph 93 as follows:

In latch circuit 800, the source terminals of  $M_1$  ~~308~~ 306,  $M_2$  ~~310~~ 308,  $M_4$  406, and  $M_7$  606 are together connected to a third node " $N_6$ " 812. In reset circuit 802, the gate and drain terminals of  $M_{12}$  804 are together connected to  $N_4$  310. The gate and drain terminals of  $M_{13}$  806 are together connected to  $N_5$  312. The source terminals of  $M_{12}$  804 and  $M_{13}$  806 are together connected to the drain terminal of  $M_{14}$  808. The drain terminal of  $M_{15}$  810 is connected to  $N_6$  812. The source terminals of  $M_{14}$  808 and  $M_{15}$  810 are together connected to analog ground  $V_{AG}$  218. (Alternatively, analog ground  $V_{AG}$  218 can be replaced by first supply voltage " $V_{SS}$ ".) Clock waveform Ck 316 is applied to the gate terminal of  $M_{14}$  808. Inverse clock waveform  $\overline{Ck}$  506 is applied to the gate terminal of  $M_{15}$  810.

***Amendments to the Drawings***

Please amend Figures 2A, 2B, and 3 according to the Request to Approve  
Proposed Drawing Corrections filed herewith.